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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yuanning Chen, et al.

Docket No: TI-35696

Serial No: 10/692,388

Conf. No: 8478

Examiner: Wai Sing Louie

Art Unit: 2814

Filed: 10/23/2003

For: ENCAPSULATED SPACER WITH LOW DIELECTRIC CONSTANT MATERIAL TO
REDUCE THE PARASITIC CAPACITANCE BETWEEN GATE AND DRAIN IN CMOS
TECHNOLOGY

ELECTION

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 3-15-05.

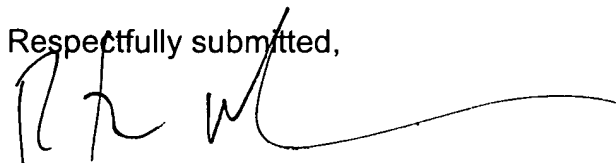

Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed February 15, 2005.

Applicants hereby elect to pursue Group I of Claims 1-14 and 21-22, drawn to a method of forming a transistor, without traversing the Examiner's restriction requirement.

Respectfully submitted,



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